WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an input/output circuit formed close to an edge of a semiconductor chip;

a functional module formed on the semiconductor chip located on a central side with regard to the input/output circuit;

an electrostatic discharge protection circuit, formed in the functional module of the semiconductor chip, configured to protect a circuit located in a downstream thereof, from being destructed by electrostatic discharge; and

bumps arranged on one of major surfaces of the semiconductor chip located close to the functional module and connected to the functional module via the electrostatic discharge protection circuit.

2. The semiconductor device according to claim 1, wherein the bumps are arranged on that one of the major surface of the semiconductor chip within an area where the functional module is formed.

3. The semiconductor device according to claim 1, wherein the bumps includes a first bump and a second bump, the first bump is connected to the functional module by a first interconnection, the second bump is connected to the functional module by a second interconnection, and the electrostatic discharge protection circuit is connected between the first

interconnection and the second interconnection.

4. The semiconductor device according to claim 1, wherein the functional module includes one of a memory device and an analog IP (analog intellectual property).

5. The semiconductor device according to claim 4, wherein the memory device includes a DRAM.

6. The semiconductor device according to claim 1, wherein the electrostatic discharge protection circuit is made of a diode.

7. A semiconductor device comprising:

an input/output circuit formed close to an edge of a semiconductor chip;

a functional module formed on the semiconductor chip located on a central side with regard to the input/output circuit;

an electrostatic discharge protection circuit, formed in the functional module of the semiconductor chip, configured to protect a circuit located in a downstream thereof, from being destructed by electrostatic discharge; and

bumps arranged in a two-dimensional manner on one of major surfaces of the semiconductor chip, that of the bumps that being located close to the functional module are connected to the functional module via the electrostatic discharge protection circuit.

8. The semiconductor device according to claim 7, wherein the bumps are arranged on that one of the major

surface of the semiconductor chip within an area where the functional module is formed.

9. The semiconductor device according to claim 7, wherein the bumps includes a first bump and a second bump, the first bump is connected to the functional module by a first interconnection, the second bump is connected to the functional module by a second interconnection, and the electrostatic discharge protection circuit is connected between the first interconnection and the second interconnection.

10. The semiconductor device according to claim 7, wherein the functional module includes one of a memory device and an analog IP (analog intellectual property).

11. The semiconductor device according to claim 10, wherein the memory device includes a DRAM.

12. The semiconductor device according to claim 7, wherein the electrostatic discharge protection circuit is made of a diode.

13. A semiconductor device comprising:

an input/output circuit formed close to an edge of a semiconductor chip;

a functional module formed on the semiconductor chip located on a central side with regard to the input/output circuit;

an electrostatic discharge protection circuit, formed close to the functional module of the semiconductor chip, configured to protect a circuit

located in a downstream thereof, from being destructed by electrostatic discharge; and

bumps arranged on one of major surfaces of the semiconductor chip located close to the functional module and connected to the functional module via the electrostatic discharge protection circuit.

14. The semiconductor device according to claim 13, wherein the bumps includes a first bump and a second bump, the first bump is connected to the functional module by a first interconnection, the second bump is connected to the functional module by a second interconnection, and the electrostatic discharge protection circuit is connected between the first interconnection and the second interconnection.

15. The semiconductor device according to claim 13, wherein the functional module includes one of a memory device and an analog IP (analog intellectual property).

16. The semiconductor device according to claim 15, wherein the memory device includes a DRAM.

17. The semiconductor device according to claim 13, wherein the electrostatic discharge protection circuit is made of a diode.

18. A semiconductor device comprising:

an input/output circuit formed close to an edge of a semiconductor chip;

a functional module formed on the semiconductor

chip located on a central side with regard to the input/output circuit;

bumps arranged on one of major surfaces of the semiconductor chip;

a package substrate connected to the semiconductor chip by the bumps;

an electrostatic discharge protection circuit, formed on a surface of the package substrate, to which the semiconductor chip is connected, and configured to protect a circuit located in a downstream thereof, from being destructed by electrostatic discharge; and

an external connection terminal provided on a surface of the package substrate, opposite to the surface to which the semiconductor chip is connected, the external connection terminal being connected to the functional module of the semiconductor chip via the electrostatic discharge protection circuit.

19. The semiconductor device according to claim 18, wherein the bumps includes a first bump and a second bump, the first bump is connected to the functional module by a first interconnection, the second bump is connected to the functional module by a second interconnection, and the electrostatic discharge protection circuit is connected between the first interconnection and the second interconnection.

20. The semiconductor device according to claim 18, wherein the functional module includes one of

a memory device and an analog IP (analog intellectual property).

21. The semiconductor device according to claim 20, wherein the memory device includes a DRAM.

22. The semiconductor device according to claim 18, wherein the electrostatic discharge protection circuit is made of a diode.

23. The semiconductor device according to claim 18, wherein the external connection terminal includes bumps.

24. A semiconductor device comprising:

an input/output circuit formed close to an edge of a semiconductor chip;

a functional module formed on the semiconductor chip located on a central side with regard to the input/output circuit;

bumps arranged on one of major surfaces of the semiconductor chip;

a package substrate connected to the semiconductor chip by the bumps;

an electrostatic discharge protection circuit, formed on a surface of the package substrate, opposite to a surface to which the semiconductor chip is connected, and configured to protect a circuit located in a downstream thereof, from being destructed by electrostatic discharge; and

an external connection terminal provided on the

surface of the package substrate, opposite to the surface to which the semiconductor chip is connected, the external connection terminal being connected to the functional module of the semiconductor chip via the electrostatic discharge protection circuit.

25. The semiconductor device according to claim 24, wherein the bumps includes a first bump and a second bump, the first bump is connected to the functional module by a first interconnection, the second bump is connected to the functional module by a second interconnection, and the electrostatic discharge protection circuit is connected between the first interconnection and the second interconnection.

26. The semiconductor device according to claim 24, wherein the functional module includes one of a memory device and an analog IP (analog intellectual property).

27. The semiconductor device according to claim 26, wherein the memory device includes a DRAM.

28. The semiconductor device according to claim 24, wherein the electrostatic discharge protection circuit is made of a diode.

29. The semiconductor device according to claim 24, wherein the external connection terminal includes bumps.

30. A semiconductor device comprising:

an input/output circuit formed close to an edge of

a semiconductor chip;

a functional module formed on the semiconductor chip located on a central side with regard to the input/output circuit;

bumps arranged on one of major surfaces of the semiconductor chip;

a package substrate connected to the semiconductor chip by the bumps;

an electrostatic discharge protection circuit, formed inside the package substrate, configured to protect a circuit located in a downstream thereof, from being destructed by electrostatic discharge; and

an external connection terminal provided on a surface of the package substrate, opposite to a surface to which the semiconductor chip is connected, the external connection terminal being connected to the functional module of the semiconductor chip via the electrostatic discharge protection circuit.

31. The semiconductor device according to claim 30, wherein the bumps includes a first bump and a second bump, the first bump is connected to the functional module by a first interconnection, the second bump is connected to the functional module by a second interconnection, and the electrostatic discharge protection circuit is connected between the first interconnection and the second interconnection.

32. The semiconductor device according to

claim 30, wherein the functional module includes one of a memory device and an analog IP (analog intellectual property).

33. The semiconductor device according to claim 32, wherein the memory device includes a DRAM.

34. The semiconductor device according to claim 30, wherein the electrostatic discharge protection circuit is made of a diode.

35. The semiconductor device according to claim 30, wherein the external connection terminal includes bumps.